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PATENT ABSTRACTS OF JAPAN(21) Application number: **62250615**(51) Intl. Cl.: **H04L 27/14**(22) Application date: **06.10.87**

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**(54) DIGITAL FM
DETECTING AND
DEMODULATING SYSTEM**

(57) Abstract:

PURPOSE: To widely open an eye pattern to obtain an excellent error characteristic by shifting the sampling time by $T/2$ (T is the bit length).

CONSTITUTION: In the transmission side, input data b_n is subjected to summation logic conversion to generate new data a_n and this data has the frequency modulated and is transmitted and in the reception side, a clock synchronizing circuit 8 is used to generate a $T/2$ bit offset sampling clock from the output of a frequency detector 4. Meanwhile, the detection output is inputted to comparators 6 and 7, and comparison levels are inputted from an input terminal 5, and the comparator 6 compares the detection output with a voltage V and the comparator 7 compares the

frequency detection output with a voltage $-V$. Comparator outputs are read into D flip flops by the clock, and reproduced data b_n is obtained by exclusive OR 10. Thus, a characteristic superior in error rate is obtained.

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